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info@isispace.nl • T +31 15 256 9018 • F: +31 15 257 3969 • IBAN: NL57RABO0118953524 BIC: RABONL2U • Reg.nr. 27293068 • VAT-nr. NL817198611B01

How to use this Option Sheet:

- Fill in the form digitally. You will need to have Adobe Acrobat reader installed (free download available at **http://get.adobe.com/reader/**).
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- Once you are ready, press the Enable Read Only button to prevent accidental changes, save the changes and send the digitally filled-in Option Sheet by email to your Sales Representative.
- If you have any questions regarding this option sheet or the fill-in procedure, please do not hesitate to contact your Sales Representative for help.

Customer Contact Information

Contact Name:	
Email Address:	
Phone Nr:	
Organization / Company / Institution	
Address:	
Address (Cont'd):	
Country:	

For ISIS Use – Leave Blank –

Order Confirmation:	
Allocated WO:	
Sales responsible:	
Project/Ref.:	

General configuration

Intended Use

◉ **Flight Model (FM) (Default)**

○ **Engineering Model (EM)**
In the case of an engineering model configuration, one red LED indicating that the CPU is powered on is placed. This LED is useful for debugging, since it shows a watchdog reset. The LED is removed in the flight model configuration in order to save power.

Motherboard Configuration

◉ **Master (Default)**
The Master configuration is used as the primary computer of the satellite. The CPU is always powered on and acts as a master on the I2C bus. The Supervisor is directly connected to the CPU and does not appear on the I2C bus.

○ **Slave**
The Slave configuration is used as a general purpose processing unit in the satellite; for example as a payload data processing and storage unit. The Supervisor is accessible on the I2C bus and controls the CPU power on/off based on I2C commands.

Basic Interface Configuration

○ **No Daughterboard**

A reduced set of I/O is available to the user:

- *1xSPI with 3xCS,*
- *1xUART,*
- *4xGPIO (excluding signals available on the CSKB).*

*These signals are made available to the user by fitting the connector **J3** in the motherboard.*

*Connector **J2** shall **not** be fitted.*

Please note that due to mechanical constraints, a daughterboard cannot be placed afterwards in this configuration.

Suitable for flight.

◉ **With Daughterboard**

*The motherboard is delivered with the connector **J2**, required to host a daughterboard.*

*Connector **J3** shall **not** be fitted.*

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Daughterboard Selection

More than one sub-option can be selected below:

(Qty)

☐ EM Daughterboard — 0

Simple daughterboard to fan-out all the I/O with standard connectors.

For development purposes only, not suitable for flight.

The height of the ISIS-OBC together with the daughterboard assembly is not optimized.

☑ FM Daughterboard — 1

Simple daughterboard to fan-out all the I/O with connectors.

Suitable for flight.

Height of the ISIS-OBC together with the daughterboard assembly is optimized.

☐ Customized Daughterboard (by ISIS) — 0

The motherboard is delivered with the connectors required to host a daughterboard.

Please contact your sales representative for further information regarding custom daughterboard designs.

☐ None (Daughterboard designed and manufactured by customer)

The motherboard is delivered with the connector required to host a daughterboard.

The customer can then build their own daughterboard design according to their specification.

The interfaces are detailed in the ISIS-OBC datasheet.

Please note that Daughterboards are sold separately and might incur on additional cost. Contact your sales representative for further information regarding pricing.

Electrical Configuration

UART Configuration

UART0 (RX0, TX0)	◉ LVCMOS 3.3V (Default)	Full duplex. Standard 3.3V levels, no buffer, no inverter.
	○ RS-232	Full duplex.

I2C Protocol and Interface Configuration

Address Mode

◉ 7-bit (Default)

○ 10-bit

On-board 3.3kΩ pull-up resistors

◉ Yes (Default for Master configuration)

○ No (Default for Slave configuration)

Supervisor Address[1] (For slave configuration only)

◉ Default (0x14)

○ Alternative

[1] Note that the CPU address is always selected by the user in software for Master and Slave configurations.

CSKB Pin-out Configuration

I2C Pin-out

I^2C Clock (SCL)	*I^2C Data (SDA)*
(•) H1-43 (Default)	(•) H1-41 (Default)
( ) H1-21 (Alternative)	( ) H1-23 (Alternative)

Main 3.3V power input[2]

- (•) H2-27 + H2-28 (Default)
- ( ) H1-48 (Alternative (GOMSPACE EPS 3.3V switched line 1))
- ( ) H1-50 (Alternative (GOMSPACE EPS 3.3V switched line 2))

Debug UART[3]

- [✔] *DTXD* H2-21 (Default)
- [✔] *DRXD* H2-22 (Default)

CSKB general purpose I/O

- [✔] *GPIO22* H1-45 (Default)
- [✔] *GPIO23* H1-46 (Default)
- [ ] *GPIO24* H2-50
- [✔] *GPIO25* H2-51 (Default)
- [ ] *GPIO26* H2-52

Important note: The list above does not detail all the CSKB pins used by the OBC. Additionally, some CSKB pins have a breakout wire connections on the OBC although these pins are not used by the OBC directly.

Please refer to the ISIS-OBC datasheet for more details.

[2] Note that pin H2-27 and H2-28 are **always** electrically connected.
[3] The debug UART is available on the programming connector and on breakout wire connections for all cases.

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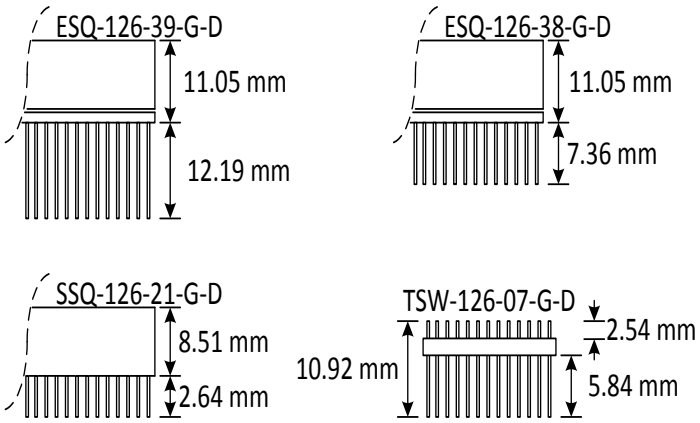
Connector type and placement



Note: The middle reference point is the top of the board. The iOBC board is 1.7mm thick.

Standard Stack Through

Other CSKB components possible on top and bottom

- (●) Samtec ESQ-126-39-G-D (Default)
- ( ) Samtec ESQ-126-38-G-D

Stack Termination Bottom

No other CSKB components possbile below the ISIS-OBC

- ( ) Samtec SSQ-126-21-G-D

Stack Termination Top

No other CSKB components possible above the ISIS-OBC

- ( ) Samtec TSW-126-07-G-D

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