# ARQ-LVD001

## RAD-HARD Quad 500 Mbps Bus LVDS Driver

### FEATURES

- 500.0 Mbps low jitter data path
- 3.3 V power supply
- LVCMOS/LVTTL compatible inputs
- Low Power Consumption
- 6 mA output driver short circuit (OUT+, OUT−)
- Cold sparing on all pins
- 2ns Propagation delay in temperature range
- Radiation tolerant: 300 krad(Si)
- Latch-up free up to 67 MeVcm$^2$/mg
- ESD tolerance: 8 kV (HBM)
- Packaging: 16 pin, Ceramic Flat Pack (FP-16).
- ANSI TIA/EIA 644a LVDS standard Compliant
- Space level

### DESCRIPTION

ARQUIMEA's ARQ-LVD001 device is a Quad Bus Low Voltage Differential Signals (LVDS) Driver intended for low power and high-speed operation.
Data path consists in LVCMOS/LVTTL input with its associated fully differential LVDS output for low noise generation and low pulse width distortion.
The ARQ-LVD001 enables high speed LVDS data transmission for point-to-point or multi-drop interconnects. This device is specially designed for the bridging of multiple backplanes in a system while consuming minimal power with reduced EMI.

In addition, the Quad LVDS Driver supports an overall TRI-STATE function that may be used to disable the output stages, disabling the load current, and thus dropping the device to an ultra-low idle power state.

All pins, including CMOS inputs, have Cold Spare capabilities. The pins will be high impedance when VDD is tied to VSS.

### APPLICATIONS

The ARQ-LVD001 provides the basic bus driver functions which allow isolation of segments or long-distance applications.

The intended application of these devices and signaling technique is for both space-wire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.
The transmission media may be printed-circuit board traces, backplanes, or cables.

### RADIATION HARDENING

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| TID | 300 | - | - | krad | |
| SEL | 67 | - | - | MeV·cm$^2$/mg | |
| BER performance | $10^{-13}$ | - | - | Err/Bit | |

More information about radiation hardening features and radiation test conditions is available under request.

### AVAILABLE OPTIONS

| PRODUCT ORDERING Nº | QUALITY LEVEL | PACKAGE (*1) | OPERATING TEMPERATURE | VARIANT DETAIL | TERMINAL MATERIAL AND FINISH (*2) | DELIVERY PACK |
|---|---|---|---|---|---|---|
| ARQ-LVD001-01 | Engineering Model (*3) | 16-pin Ceramic FP | -55ºC to 125ºC | NA | D2 | 15-pieces tray |
| ARQ-LVD001S01 | Space Flight Model (*4) | 16-pin Ceramic FP | -55ºC to 125ºC | NA | D2 | 15-pieces tray |

(*1) Other packaging options, including raw die format, are also available under request.
(*2) The terminal material and/or finish shall be in accordance with the requirements of ESCC23500
(*3) Only electrically tested at 25ºC
(*4) Space level screening and qualification per ESCC9000

## INDEX



## GLOSSARY

| | |
|---|---|
| ***BER*** | *Bit Error Ratio* |
| ***CMRR*** | *Common Mode Rejection Ratio* |
| ***CQFP*** | *Ceramic Quad Flat Pack* |
| ***ESD*** | *Electrostatic Discharge* |
| ***GEO*** | *Geostationary Earth Orbit* |
| ***IC*** | *Integrated Circuit* |
| ***I/O*** | *Input/Output* |
| ***LET*** | *Linear Energy Transfer* |
| ***LVDS*** | *Low Voltage Differential Signaling* |
| ***LVTTL*** | *Low Voltage Transistor-Transistor Logic* |
| ***PSRR*** | *Power Supply Rejection Ratio* |
| ***RL*** | *Load Resistor* |
| ***SEE*** | *Single Event Effect* |
| ***SEL*** | *Single Event Latch-up* |
| ***TID*** | *Total Ionizing Dose* |
| ***tf*** | *Fall Time* |
| ***tr*** | *Rise Time* |
| ***TTL*** | *Transistor-Transistor Logic* |
| ***VCM*** | *Common-mode voltage* |
| ***VID*** | *Differential Input Voltage* |
| ***VOS*** | *Offset voltage* |
| ***VT*** | *Differential output voltage* |

## OVERVIEW

The ARQ-LVD001 provides the basic driver function. The device operates as a Quad Driver LVDS, generating a LVDS signal from a CMOS/TTL input.
The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

## BLOCK DIAGRAM

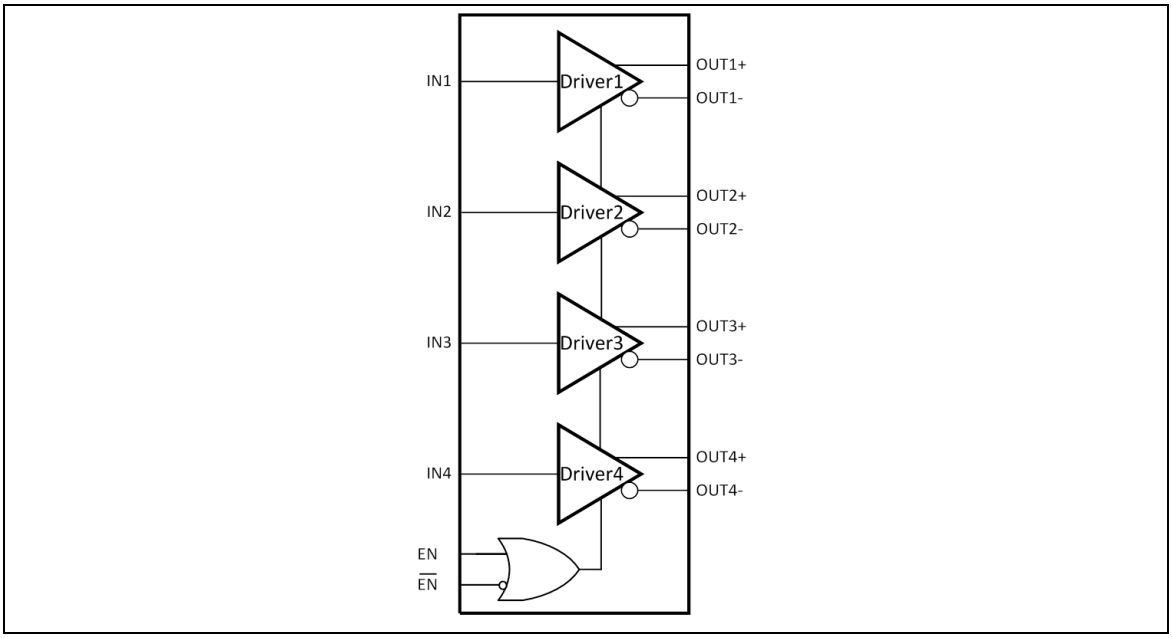



**Figure 1: Block diagram**

## TRUTH TABLE

| MODE | ENABLES | | INPUTS | OUTPUTS | |
|---|---|---|---|---|---|
| | EN | EN/ | IN | OUT+ | OUT- |
| Disabled | L or OPEN | H | X | Z | Z |
| Enabled | H | X | L | L | H |
| | H | X | H | H | L |
| | H | X | OPEN | L | H |
| | X | L or OPEN | L | L | H |
| | X | L or OPEN | H | H | L |
| | X | L or OPEN | OPEN | L | H |

**Table 1: Driver Truth table**

Notes:
(*) L= low Logic Level, H= High Logic Level, X= Irrelevant (L, OPEN or H), Z= High Impedance

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | VALUE |
|---|---|---|
| $V_{DD}$ | DC supply voltage | -0.5 V to 4.6 V |
| $V_I$ | TTL/CMOS Input Voltage | -0.5 V to 6 V |
| $T_{STG}$ | Storage temperature | -65°C to +150°C |
| $T_J$ | Maximum junction temperature | +175°C |
| Tc | Maximum Case temperature | +125°C |
| ESD | ESD Last Passing Voltage – HBM | 8 kV |
| $P_D$ | Power dissipation | 200 mW |

**Table 2: Absolute Maximum Rating**

Note: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

## RECOMMENDED OPERATING CONDITIONS

The Recommended Operating as well as derated Conditions according to ECSS-Q-30-11A are presented below:

| SYMBOL | PARAMETER | OPERATING VALUES | DERATED VALUES |
|---|---|---|---|
| $V_{DD}$ | Power supply voltage | 3.0 V to 3.6 V | 3.0 V to 3.6 V |
| $V_{IN}$ | DC input voltage, logic inputs (EN or EN/) | 0 V to 5 V | 0 V to 5 V |
| $T_C$ | Case temperature range | -55°C to +125°C | +100ºC (Tj=110ºC) |

**Table 3: Recommended Operating Conditions**

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, -55°C < TC < +125°C

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **TTL/CMOS DC SPECIFICATIONS (EN, ENn and IN)** | | | | | |
| $V_{IH}$ | High-level input voltage | | 2.0 | 5 | V |
| $V_{IL}$ | Low-level input voltage | | -0.3 | 0.8 | V |
| $I_{IH}$ | High-level input current | $V_{DD}$ = 3.6V, $V_{IN}$ = 3.6V; | -10 | +10 | µA |
| $I_{IL}$ | Low-level input current | $V_{DD}$ = 3.6V, $V_{IN}$ = 0V | -10 | +10 | µA |
| $I_{CS}$ | Cold Spare Leakage current | $V_{DD}$ = $V_{SS}$, $V_{IN}$ = 3.6V | -3,6 | +3,6 | µA |
| **LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)** | | | | | |
| $V_{OD}$ | Differential Output Voltage | $R_L$ = 100 Ω | 247 | 454 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between complementary output states | $R_L$ = 100 Ω | | 10 | mV |
| $V_{OS}$ | Offset Voltage | $R_L$ = 100 Ω $V_{OS} = \frac{V_{OH}+V_{OL}}{2}$ | 1.125 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between complementary output states | $R_L$ = 100 Ω | | 50 | mV |
| $\Delta V_{OSB}$ | Imbalance of Differential Offset Voltage during Voltage transition | $R_L$ = 100Ω, $C_L$ = 1 to 10pf | | 150 | mV |
| $I_{OZ}$ | Output Tri-State Current | Tri-State output (channel disabled), $V_{OUT}$ = $V_{DD}$ or $V_{SS}$ | -5 | +5 | µA |
| $I_{CSOUT}$ | Cold Sparing Leakage Current | $V_{DD}$ = $V_{SS}$, $V_{OUT}$ = 3.6V | -5 | +5 | µA |
| $I_{OS}$ | Output Short Circuit Current (Only one output should be shorted at a time) | $V_{OUT+}$=$V_{OUT-}$=0V | 6 | 24 | mA |
| | | $V_{OUT+}$=$V_{OUT-}$ | 4 | 12 | mA |
| **SUPPLY CURRENT** | | | | | |
| $I_{CLLS}$ | Total Supply Current | $R_L$ = 100 Ω, ENn = $V_{SS}$, EN = $V_{DD}$, $V_{DD}$ = 3.6 V, Fq = DC | | 30 (23 typ) | mA |
| $I_{CCZ}$ | Tri-State Supply Current | $R_L$=100Ω, ENn = $V_{DD}$, EN = $V_{SS}$, $V_{DD}$ = 3.6 V | | 10 (6 typ) | mA |
| PSRR | Power Supply Rejection Ratio | $R_L$=100Ω, ENn = $V_{SS}$, EN = $V_{DD}$, $V_{DD}$=3.6V, Fq=250MHz Power supply Fq=1MHz | | -50 | dB |

**Table 4: DC Electrical Characteristics**

## AC SWITCHING CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3 V ± 0.3 V, TA = -55°C to +125°C.

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{PHZ}$ | Disable Time (Active to Tri-State) High to Z | $R_L$ = 100 Ω, $C_L$ = 10 pf | | 4.5 | ns |
| $t_{PLZ}$ | Disable Time (Active to Tri-State) Low to Z | $R_L$ = 100 Ω, $C_L$ = 10 pf | | 4.5 | ns |
| $t_{PZH}$ | Enable Time (Tri-State to Active) Z to High | $R_L$ = 100 Ω, $C_L$ = 10 pf | | 250 | ns |
| $t_{PZL}$ | Enable Time (Tri-State to Active) Z to Low | $R_L$ = 100 Ω, $C_L$ = 10 pf | | 250 | ns |
| $t_{LHT}$ | Input/Output Low-to-High Transition Time, 20% to 80% | $R_L$ = 100 Ω, $C_L$ = 1 to 10pf | 260 | 600 | ps |
| $t_{HLT}$ | Input/Output High-to-Low Transition Time, 80% to 20% | $R_L$ = 100 Ω, $C_L$ = 1 to 10pf | 260 | 600 | ps |
| $t_{PLHD}$ | Propagation Low to High Delay | $R_L$ = 100 Ω, $C_L$ = 10pf | | 2 | ns |
| $t_{PHLD}$ | Propagation High to Low Delay | $R_L$ = 100 Ω, $C_L$ = 10pf | | 2 | ns |
| $T_{SKEW}$ | Differential Skew | $t_{PHLD}$ - $t_{PLHD}$ | | 150 | ps |
| $T_{CCS}$ | Output Channel-to-Channel Skew | $R_L$ = 100 Ω, $C_L$ = 10pf | | 500 | ps |
| $T_{DDS}$ | Output Device-to-Device Skew | $R_L$ = 100 Ω, $C_L$ = 10pf | | 750 | ps |
| $t_{PJ}$ | Periodic Jitter | 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%) | | 15 | ps |
| $t_{CCJ}$ | Cycle to Cycle Jitter | 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%) | | 40 | ps |
| $t_{PPJ}$ | Peak to Peak Jitter | $V_{IN}$ = 2^(7)-1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%) | | 250 | ps |
| $t_{DJ}$ | Deterministic Jitter | $V_{IN}$ = 2^(7)-1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%) | | 200 | ps |

**Table 5: AC Electrical Characteristics**

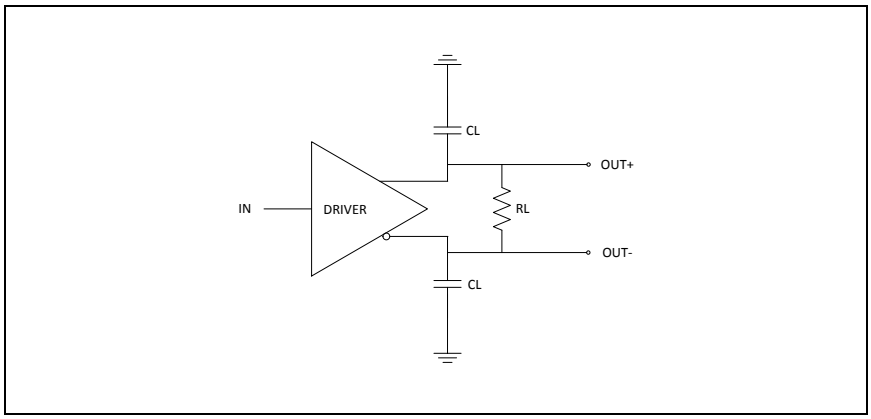



**Figure 2: LVDS Output load**

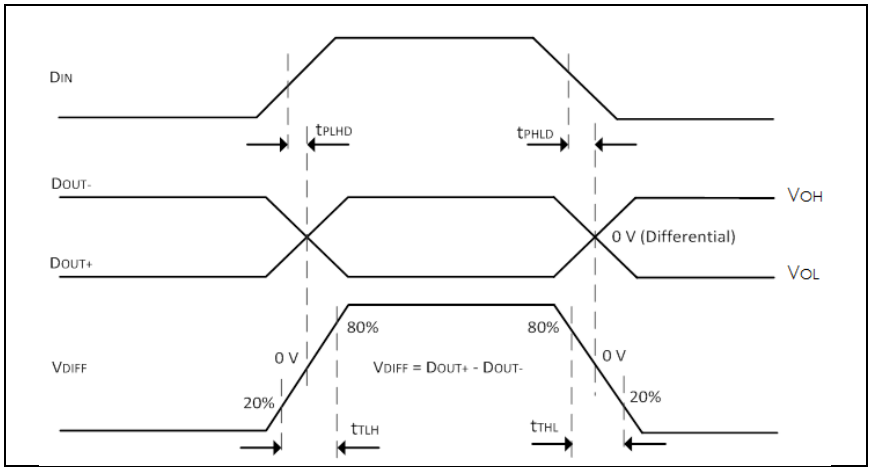



**Figure 3: LVDS Propagation delay and transition time**

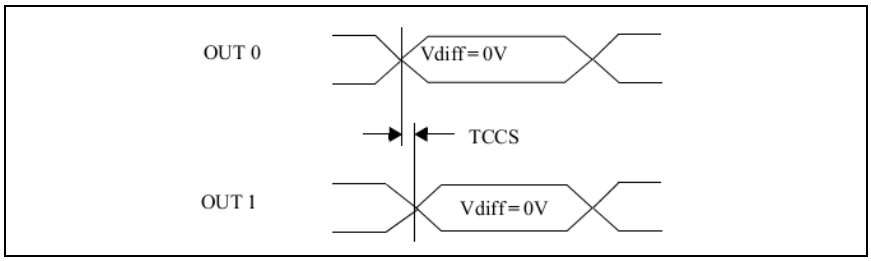



**Figure 4: Output channel to channel skew**

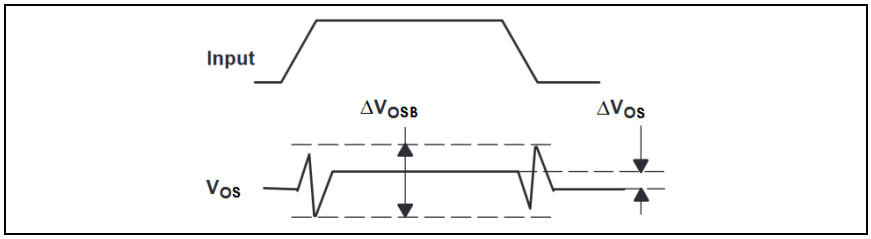
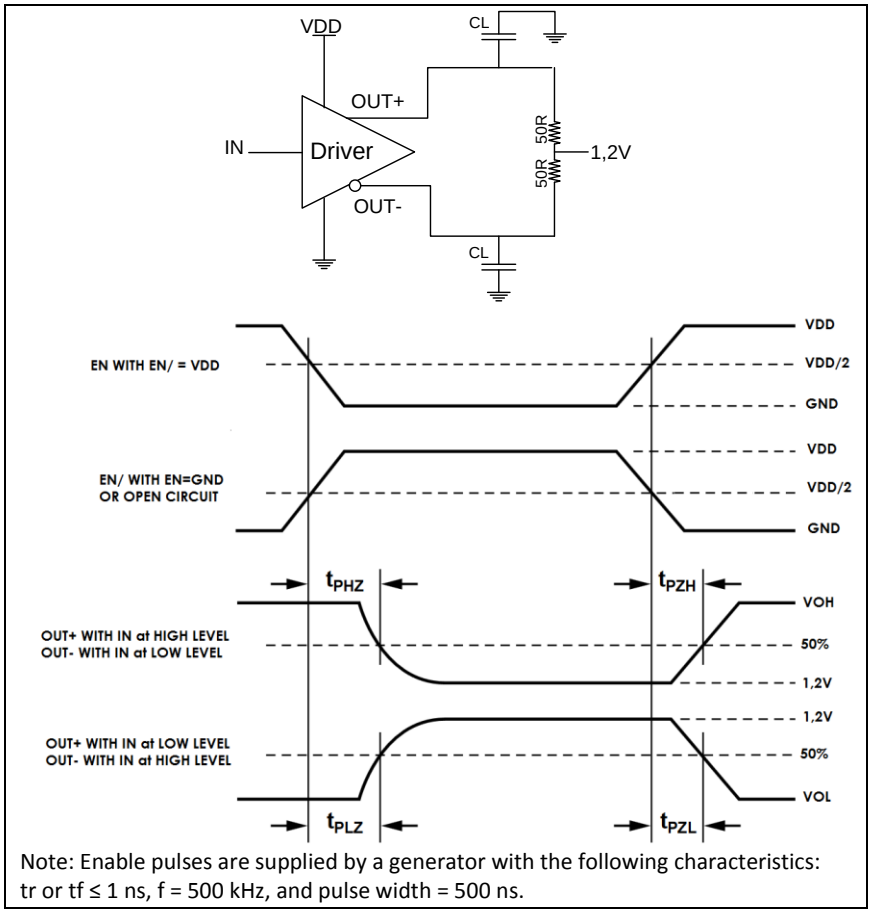



**Figure 5: LVDS Offset Voltage**




Note: Enable pulses are supplied by a generator with the following characteristics: tr or tf ≤ 1 ns, f = 500 kHz, and pulse width = 500 ns.

**Figure 6: Output active to TRISTATE and TRISTATE to active**

## APPLICATIONS INFORMATION

### *Transmission media:*

The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The signal path should be matched in length to avoid any skew in differential lines or between channels.

### *PCB layout and Power System Bypass:*

Circuit board layout and stack-up for the ARQ-LVD001 should be designed to provide noise-free power to the device.

Good layout practice also will separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. A 0.25 Ω resistor is recommended in the power supply line path. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use value of 0.1 µF. Tantalum capacitors may be 2.2 µF. Voltage rating for tantalum capacitors should be at least 5x the power supply voltage being used. It is recommended practice to use two vias at each power pin of the ARQ-LVD001, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

## PINOUT DESCRIPTION

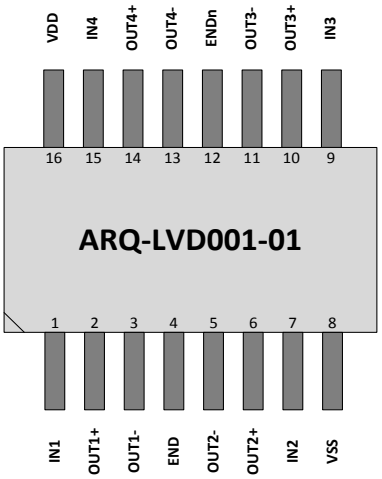



**Figure 7: Pinout diagram**

| Pin Nº | Name | Type | Description |
|---|---|---|---|
| 1 | IN1 | Digital Input | CMOS/TTL input, channel 1 |
| 2 | OUT1+ | LVDS Output | Non-Inverting LVDS output, channel 1 |
| 3 | OUT1- | LVDS Output | Inverting LVDS output, channel 1 |
| 4 | END | Digital Input | Logic enable for the LVDS |
| 5 | OUT2- | LVDS Output | Inverting LVDS output, channel 2 |
| 6 | OUT2+ | LVDS Output | Non-Inverting LVDS output, channel 2 |
| 7 | IN2 | Digital Input | CMOS/TTL input, channel 2 |
| 8 | VSS | Power | Ground |
| 9 | IN3 | Digital Input | CMOS/TTL input, channel 3 |
| 10 | OUT3+ | LVDS Output | Non-Inverting LVDS output, channel 3 |
| 11 | OUT3- | LVDS Output | Inverting LVDS output, channel 3 |
| 12 | ENDn | Digital Input | Logic active low enable for the LVDS |
| 13 | OUT4- | LVDS Output | Inverting LVDS output, channel 4 |
| 14 | OUT4+ | LVDS Output | Non-Inverting LVDS output, channel 4 |
| 15 | IN4 | Digital Input | CMOS/TTL input, channel 4 |
| 16 | VDD | Power | 3.3 V Power |

**Table 6: Pinout description**

## PACKAGE

### *FP16 Drawing*

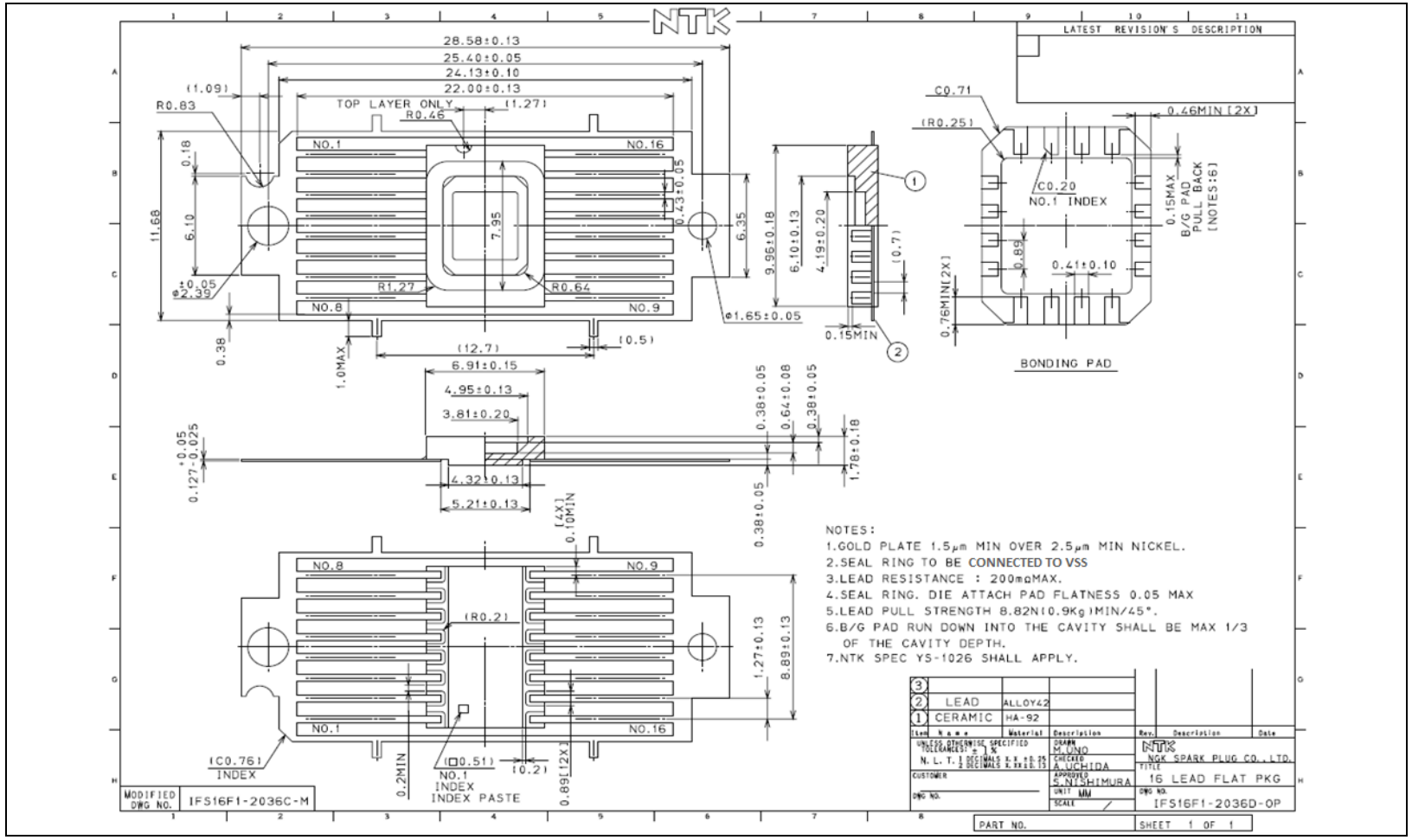



**Figure 8: FP-16 Package drawing**

Notes:
1. An Index mark shall be located adjacent to Pin 1.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centerlines. Each pin centerline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
5. The lid is electrically connected to VSS.
6. Lead finishes are in accordance to MIL-PRF-38535.

## MARKING

The laser marked information on the component are:

- ARQUIMEA's symbol **Q**
- The Entire Part-type
- Traceability information

The traceability information comprises a manufacturing date code, a lot identification and a serial number:

- **Date Code**: Four-digit code number is used for the manufacturing date. The first two digits are the last two figures of the year of manufacture. The last two digits indicate the week of the year (i.e. 01 to 52), during which encapsulation or the final production process occurred.

- **Lot and Selected Sublot Identification**: If it is necessary to differentiate between more than one lot processed in the same week, a suffix letter (beginning with the letter A) is added to the date code. For a Selected Sublot a second suffix letter (beginning with the letter A) is added to the date code. For a single lot or sublot, letters are omitted (replaced by space).
- **Serial Number**: A serial number consisting of three digits is used. Serial numbers are run sequentially and not duplicated if more than one sub-lot is taken from one production lot.

For Engineering Models, "**EM**" marking is written after Serial Number

## QUALITY STANDARDS

ARQUIMEA INGENIERÍA S.L.U. develops its activities under the premises of quality and sustainability, offering efficient, liable and innovative technologies and solutions to its customers.

ARQUIMEA's Quality Management System meets the requirements of ISO 9100:2010 Aerospace Series and has been audited and certified by the Spanish Association for Standardization and Certification, AENOR.


To meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in the following processes (Screened and Qualified):

- Equivalent to QML 38535 LEVEL Q or V* (on request)
- Equivalent to ESCC 9000*

  *with radiation Qualification

For the procurement in die form, the following processes can be offered on request:

- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K*

Engineering Models are available and tested at 25ºC only.

## IMPORTANT NOTICE

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**REVISION HISTORY**

| Date Released | Issue | Section | Changes |
|---|---|---|---|
| 04-04-2016 | Draft A | All | Initial Release. |
| 23-09-2016 | Draft B | ELECTRICAL CHARACTERISTICS<br>AC SWITCHING CHARACTERISTICS | Parameter update after electrical Measurements |
| 19-10-2016 | Draft C | ELECTRICAL CHARACTERISTICS<br>AC SWITCHING CHARACTERISTICS | Jitter and PSRR parameters added |
| 19-05-2017 | Draft D | ELECTRICAL CHARACTERISTICS | $I_{CLLS}$ parameter added |
| 19-09-2017 | Draft E | All<br>ELECTRICAL CHARACTERISTICS | Minor rewording<br>Parameter update after Electrical Measurements |
| 30-10-2017 | Issue 01 | ELECTRICAL CHARACTERISTICS | Capacitive load from 1 to 10pF for transition time tests |
| 18-12-2017 | Issue 02 | TRUTH TABLE | Added table |
| 20-02-2018 | 03 | AVAILABLE OPTIONS<br>PACKAGE<br>MARKING | Added description<br>Notes Added<br>Added Information |
| 01-07-2018 | 04 | ELECTRICAL CHARACTERISTICS | Parameter update after electrical measurements |

Space Technology Partner

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