

**ARQ-LVP001****RAD-HARD Octal 500 Mbps Bus LVDS Repeater****FEATURES**

- 500.0 Mbps low jitter fully differential data path
- 250 MHz clock channel
- 3.3V power supply
- LVCMOS/LVTTL compatible inputs
- Low power consumption
- 6mA output driver short circuit (OUT+, OUT-)
- Cold sparing on all pins
- 3.5ns Propagation delay in temperature range
- Extended LVDS Input Common Mode [-4; +5] V
- Receiver input threshold  $\leq \pm 100$  mV
- 25mV (typ.) Input hysteresis
- Fail-safe protection circuit
- Radiation tolerant: 300 Krad(Si)
- Latch-up free up to 60 MeVcm<sup>2</sup>/mg
- ESD tolerance: 8KV
- Packaging: 48-pin Ceramic Quad Flat Pack (CQFP)
- ANSI TIA/EIA 644a LVDS Standard Compliant
- Space level

**DESCRIPTION**

ARQUIMEA's ARQ-LVP001 device is an Octal Bus Low Voltage Differential Signals (LVDS) Repeater intended for low power and high-speed operation. Data path is fully differential from input to output for low noise generation and low pulse width distortion. The ARQ-LVP001 allows high speed data transmission for point-to-point or multi-drop interconnects. It is specifically designed for the bridging of multiple backplanes in a system while consuming minimal power with reduced EMI.

**RADIATION HARDENING**

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
TID	300	-	-	Krad	Only validated on former design ARQ-LVR001
SEL	60	-	-	MeVcm <sup>2</sup> /mg	
SEE performance for a GEO orbit	1E-13	-	-	Err/Bit	

More information about radiation hardening features and radiation test conditions is available under request.

**AVAILABLE OPTIONS**

PRODUCT ORDERING Nº	QUALITY LEVEL	PACKAGE (*1)	OPERATING TEMPERATURE	VARIANT DETAIL	TERMINAL MATERIAL AND FINISH (*2)	DELIVERY PACK
ARQ-LVP001-03	Engineering Model (*3)	48 pin CQFP	-55°C to 125°C	NA	D2	15-pieces tray
ARQ-LVP001S03	Space Flight Model (*4)	48 pin CQFP	-55°C to 125°C	NA	D2	15-pieces tray

(\*1) Other packaging options, including raw die format, are also available under request.

(\*2) The terminal material and/or finish shall be in accordance with the requirements of ESCC23500

(\*3) Only electrically tested at 25°C

(\*4) Space level screening and qualification per ESCC9000

The Octal LVDS Repeater supports an overall TRI-STATE function that may be used to disable the output stages, disabling the load current, and thus dropping the device to an ultra-low idle power state.

All pins, including CMOS Input, have Cold Spare buffers. The pins will be high impedance when VDD is tied to VSS.

The input buffers of LVDS receiver include an active internal fail-safe circuit that sets the output of the receiver to a known high state when one or the two inputs floating or inputs shorted.

The extended common mode range allows high voltage drops between ground planes without affecting performance.

**APPLICATIONS**

The ARQ-LVP001 provides the basic bus repeater function. The device operates as a 9 channel LVDS buffer (including Clock) repeating the signal, restoring the LVDS amplitude, allowing to drive another media segment, allowing isolation of segments or long-distance applications.

The intended application of these devices and signaling technique is for both space-wire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

The transmission media may be printed-circuit board traces, backplanes, or cables.

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## GLOSSARY

<b>BER</b>	<i>Bit Error Ratio</i>
<b>CMRR</b>	<i>Common Mode Rejection Ratio</i>
<b>CQFP</b>	<i>Ceramic Quad Flat Pack</i>
<b>ESD</b>	<i>Electrostatic Discharge</i>
<b>GEO</b>	<i>Geostationary Earth Orbit</i>
<b>IC</b>	<i>Integrated Circuit</i>
<b>I/O</b>	<i>Input/Output</i>
<b>LET</b>	<i>Linear Energy Transfer</i>
<b>LVDS</b>	<i>Low Voltage Differential Signaling</i>
<b>LVTTL</b>	<i>Low Voltage Transistor-Transistor Logic</i>
<b>PSRR</b>	<i>Power Supply Rejection Ratio</i>
<b>RL</b>	<i>Load Resistor</i>
<b>SEE</b>	<i>Single Event Effect</i>
<b>SEL</b>	<i>Single Event Latch-up</i>
<b>TID</b>	<i>Total Ionizing Dose</i>
<b>tf</b>	<i>Fall Time</i>
<b>tr</b>	<i>Rise Time</i>
<b>TTL</b>	<i>Transistor-Transistor Logic</i>
<b>VCM</b>	<i>Common-mode voltage</i>
<b>VID</b>	<i>Differential Input Voltage</i>
<b>VOS</b>	<i>Offset voltage</i>
<b>VT</b>	<i>Differential output voltage</i>

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OVERVIEW

The ARQ-LVP001 provides the basic bus repeater function. The device operates as a 9 channel LVDS buffer. Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long-distance applications. The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

BLOCK DIAGRAM

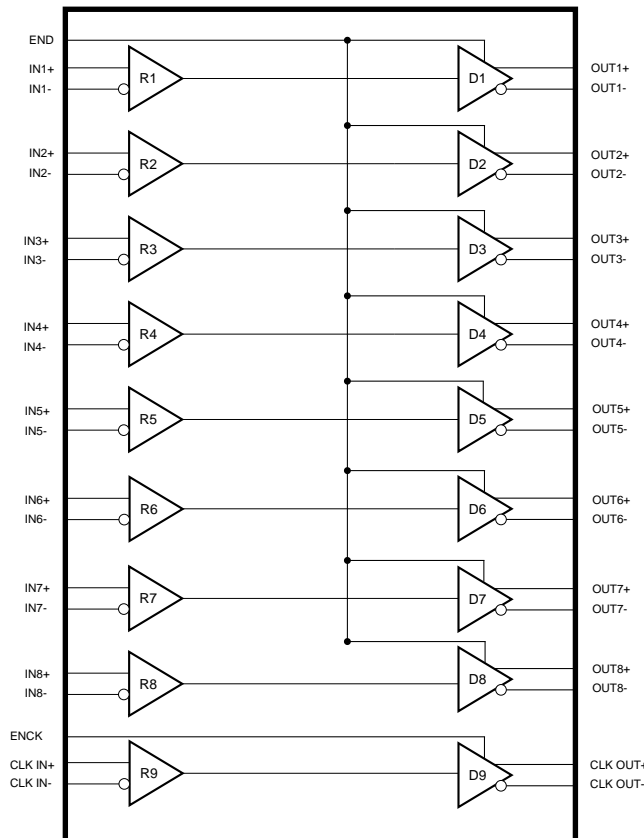


Figure 1: Block diagram

TRUTH TABLE

MODE	ENABLE	INPUTS	OUTPUTS	
	END or ENCK	$V_{ID} = V_{IN+} - V_{IN-}$	OUT+	OUT-
Disabled	L	X	Z	Z
Enabled	H	$V_{ID} > V_{TH}$	H	L
		$V_{TL} < V_{ID} < V_{TH}$	?	?
		$V_{ID} < V_{TL}$	L	H
Fail-Safe	H	OPEN/SC/Terminated for $t_{FS} > 500ns$	H	L

Table 1: Truth table

Notes:

(\*) L= low Logic Level, H= High Logic Level, X= Irrelevant, Z= High Impedance, '?'=Indeterminate

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**ABSOLUTE MAXIMUM RATINGS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>VALUE</b>
V <sub>DD</sub>	DC supply voltage	-0.5 to 4.6V
V <sub>i</sub>	TTL/CMOS Input Voltage	-0.5V to 6V
V <sub>IN</sub>	LVDS Input Voltage	-5V to 6V
T <sub>STG</sub>	Storage temperature	-65 to +150°C
T <sub>J</sub>	Maximum junction temperature	+175°C
T <sub>C</sub>	Maximum Case temperature	+125°C
ESD	ESD Last Passing Voltage – HBM	8kV
P <sub>D</sub>	Power dissipation	1W

**Table 2: Absolute Maximum Rating**

Note: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

**RECOMMENDED OPERATING CONDITIONS**

The Recommended Operating as well as derated Conditions according to ECSS-Q-30-11A are presented below

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>OPERATION VALUES</b>	<b>DERATED VALUES</b>
V <sub>DD</sub>	Power supply voltage	3.0 to 3.6V	3.0 to 3.6V
V <sub>IN</sub>	TTL/CMOS input voltage	0 to 5V	0 to 5V
	LVDS input voltage, receiver inputs	-4.6V to 5.6V	-4.6V to 5.6V
V <sub>CM</sub>	LVDS Input Common Mode Voltage	-4V to 5V	-4V to 5V
T <sub>C</sub>	Case temperature range	-55 to +125 °C	+100°C (T <sub>J</sub> =110°C)

**Table 3: Recommended Operating Conditions**

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**ELECTRICAL CHARACTERISTICS**Unless otherwise stated, these specifications apply for  $V_{DD} = 3.3V \pm 0.3V$ ,  $-55^{\circ}C < TC < +125^{\circ}C$ 

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
<b>TTL/CMOS DC SPECIFICATIONS (EN, ENK)</b>					
$V_{IH}$	High-level input voltage		2.0	5V	V
$V_{IL}$	Low-level input voltage		-0.3	0.8	V
$I_{IH}$	High-level input current	$V_{DD} = 3.6V, V_{IN} = 3.6V$	-10	+10	$\mu A$
$I_{IL}$	Low-level input current	$V_{DD} = 3.6V, V_{IN} = 0V$	-10	+10	$\mu A$
$I_{CS}$	Cold Spare Leakage current	$V_{DD} = V_{SS}, V_{IN} = 3.6V$	-3,6	+3,6	$\mu A$
<b>LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)</b>					
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	247	453	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between complementary output states	$R_L = 100\Omega$		10	mV
$V_{OS}$	Offset Voltage	$R_L = 100\Omega, V_{OS} = \frac{V_{OH} + V_{OL}}{2}$	1.125	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between complementary output states	$R_L = 100\Omega$		50	mV
$\Delta V_{OSB}$	Imbalance of Differential Offset Voltage during Voltage transition	$R_L = 100\Omega, C_L = 1pf \text{ to } 10pF$		150	mV
$I_{OZ}$	Output Tri-State Current	Tri-State output (channel disabled), $V_{OUT} = V_{DD} \text{ or } V_{SS}$	-5	+5	$\mu A$
$I_{CSOUT}$	Cold Sparing Leakage Current	$V_{DD} = V_{SS}, V_{OUT} = 3.6V,$	-5	+5	$\mu A$
$I_{OS}$	Output Short Circuit Current (Only one output should be shorted at a time)	$V_{OUT+}=V_{OUT-}=0V$	6	24	mA
		$V_{OUT+}=V_{OUT-}$	4	12	mA
<b>LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)</b>					
$V_{TH}$	Differential Input High Threshold	$V_{CM} = -4V \text{ to } +5V$	+100	+600	mV
$V_{TL}$	Differential Input Low Threshold	$V_{CM} = -4V \text{ to } +5V$	-600	-100	mV
$V_{ID\_HYS}$	Differential Input hysteresis ( $V_{TH} - V_{TL}$ )	$V_{CM} = -4V \text{ to } +5V$	15		mV
$V_{FSH}$	Differential Input Fail-Safe High Threshold	$V_{CM1} = -4V \text{ to } +5V,$ Hold time>500ns	+10		mV
$V_{FSL}$	Differential Input Fail-Safe Low Threshold	$V_{CM1} = -4V \text{ to } +5V,$ Hold time>500ns		-10	mV
$V_{ID\_FS}$	Differential Input Fail-safe threshold	$V_{FSH} - V_{FSL}$	20		mV
$V_{CMR}$	Common Mode Voltage Range	$V_{ID} = \pm 200mV (400mVpp)$	-4	+5	V
$I_{IN}$	LVDS Input Current	$V_{DD} = +3.6V, V_{CM1} = +1.2V,$ $V_{ID} = \pm 400mV$	-10	+10	$\mu A$
		$V_{DD} = +3.6V, V_{CM1} = -4V \text{ to } +5V,$ $V_{IN+}=V_{IN-}=V_{CM1}$	-60	+60	$\mu A$
$\Delta I_{IN}$	Input Current Balance ( $I_{IN+}-I_{IN-}$ )	$V_{DD} = +3.6V, V_{CM} = -4V \text{ to } +5V,$ $V_{IN+}=V_{IN-}=V_{CM}$	-6	6	$\mu A$
$I_{CSIN}$	Cold Sparing Leakage Current	$V_{DD} = V_{SS}, V_{CM1} = +1.2V,$ $V_{ID} = \pm 400mV$	-20	+20	$\mu A$
		$V_{DD} = V_{SS}, V_{CM1} = -4V \text{ to } +5V,$ $V_{IN+}=V_{IN-}=V_{CM1}$	-60	+60	$\mu A$
$C_{IN}$	Input Capacitance			3	pF
<b>SUPPLY CURRENT</b>					
$I_{CLS}$	Total Supply Current	$R_L=100\Omega, END/ENCK=V_{DD},$ $V_{DD}=3.6V, Fq=DC$		130	mA
$I_{CCZ}$	Tri-State Supply Current	$R_L=100\Omega, END, ENCK = V_{SS},$ $V_{DD} = 3.6V$		10	mA
PSRR	Power Supply Rejection Ratio	$R_L=100\Omega, END/ENCK=V_{DD},$ $V_{DD}=3.6V, Fq=250MHz$ Power supply Fq=1MHz		-50	dB

Table 4: DC Electrical Characteristics

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AC SWITCHING CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, TA = -55°C to +125°C.

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
t <sub>PHZ</sub>	Disable Time (Active to Tri-State) High to Z	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		4.5	ns
t <sub>PLZ</sub>	Disable Time (Active to Tri-State) Low to Z	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		4.5	ns
t <sub>PZH</sub>	Enable Time (Tri-State to Active) Z to High	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		250	ns
t <sub>PZL</sub>	Enable Time (Tri-State to Active) Z to Low	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		250	ns
t <sub>LHT</sub>	Input/Output Low-to-High Transition Time, 20% to 80%	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 1pf to 10pF	260	600	ps
t <sub>HLT</sub>	Input/Output High-to-Low Transition Time, 80% to 20%	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 1pf to 10pF	260	600	ps
t <sub>PLHD</sub>	Propagation Low to High Delay	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		3,5	ns
t <sub>PHLD</sub>	Propagation High to Low Delay	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		3,5	ns
T <sub>SKREW</sub>	Differential Skew	T <sub>PHLD</sub> - T <sub>PLHD</sub>		150	ps
T <sub>CCS</sub>	Output Channel-to-Channel Skew	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10pf		500	ps
T <sub>DDS</sub>	Output Device-to-Device Skew	R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 10pf		750	ps
t <sub>PJ</sub>	Periodic Jitter	V <sub>ID</sub> =±200mV (400mVpp), 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		15	ps
t <sub>CCJ</sub>	Cycle to Cycle Jitter	V <sub>ID</sub> =±200mV (400mVpp), 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		40	ps
t <sub>PPJ</sub>	Peak to Peak Jitter	V <sub>ID</sub> = 2 <sup>(7)</sup> -1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		250	ps
t <sub>DJ</sub>	Deterministic Jitter	V <sub>ID</sub> = 2 <sup>(7)</sup> -1 PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		200	ps

Table 5: AC Electrical Characteristics

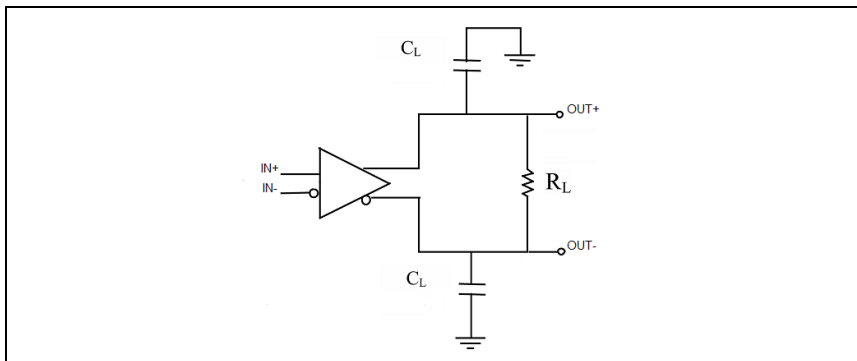


Figure 2: LVDS Output load

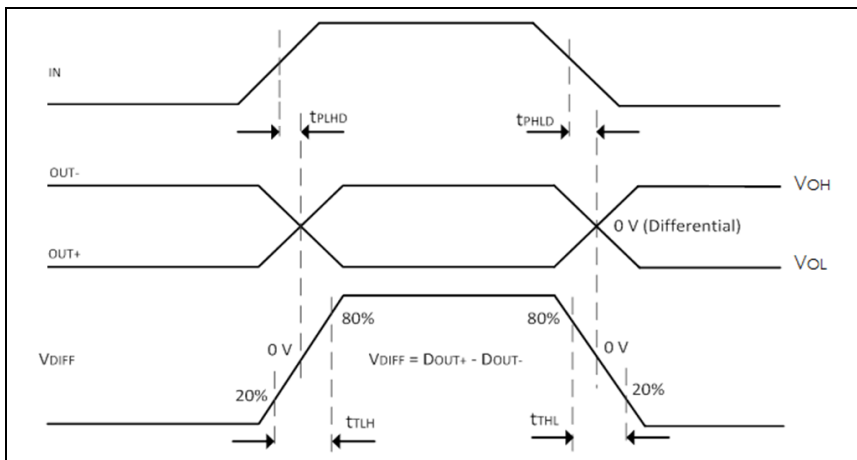


Figure 3: LVDS propagation delay and Output Transition time

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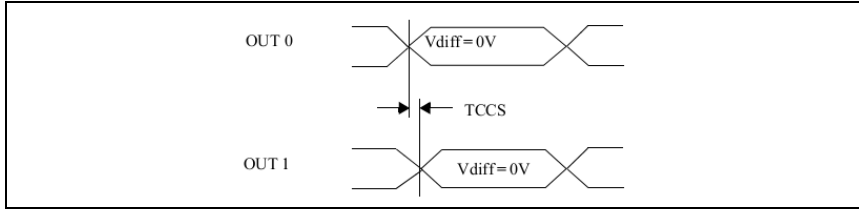


Figure 4: Output channel to channel skew

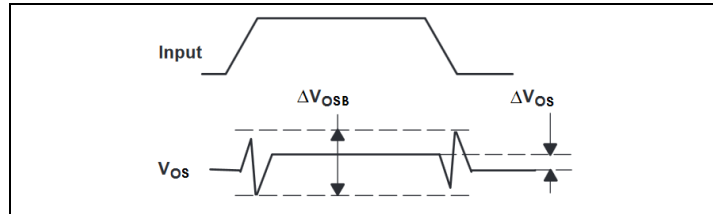


Figure 5: LVDS Offset Voltage

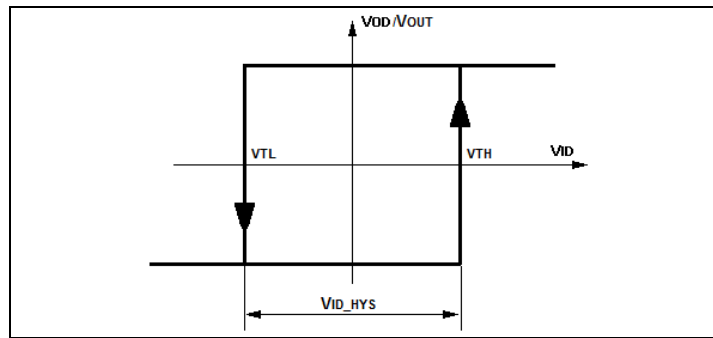


Figure 6: Input Differential Hysteresis

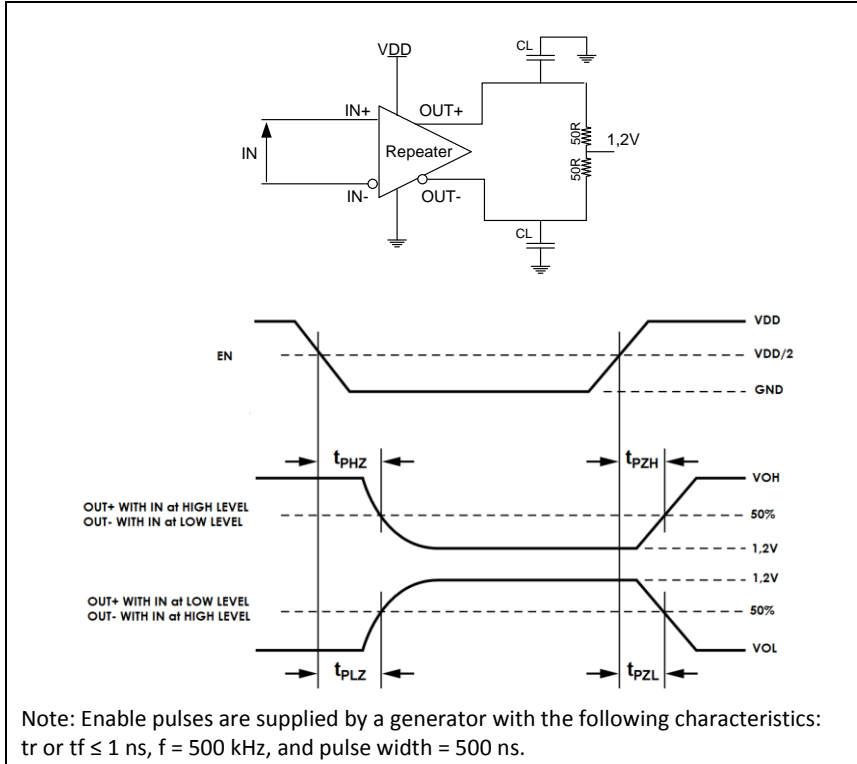


Figure 7: Output active to TRISTATE and TRISTATE to active





## APPLICATIONS INFORMATION

### **Transmission media:**

The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The signal path should be matched in length to avoid any skew in differential lines or between channels.

### **Input Fail-Safe** (comparator and timer):

The ARQ-LVP001 also supports Fail-Safe operation when OPEN or SHORTED inputs are present. Receiver output goes HIGH after 500ns for all fail-safe conditions.

### **PCB layout and Power System Bypass:**

Circuit board layout and stack-up for the ARQ-LVP001 should be designed to provide noise-free power to the device.

Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less

critical. A 0.250ohm resistor is recommended in the power supply line path. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use value of 0.1 $\mu$ F. Tantalum capacitors may be 2.2 $\mu$ F. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the ARQ-LVP001, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

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PINOUT DESCRIPTION

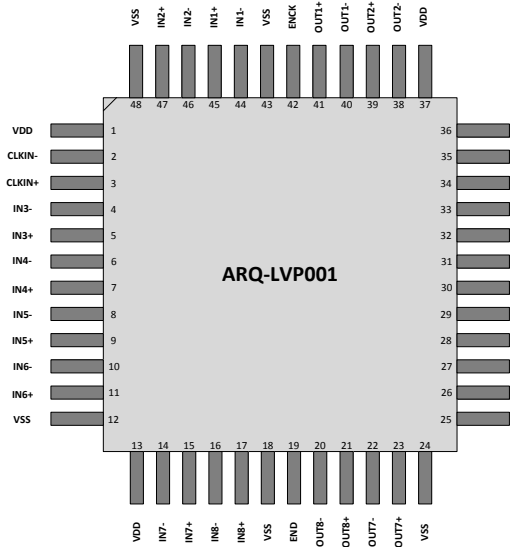


Figure 8: Pinout diagram

Nº pin	Name	Type	Description
5, 7, 9, 11, 15, 17, 45, 47	INn+	LVDS Input	Non-Inverting LVDS input
4, 6, 8, 10, 14, 16, 44, 46	INn-	LVDS Input	Inverting LVDS input
21, 23, 27, 29, 31, 33, 39, 41	OUTn+	LVDS Output	Non-Inverting LVDS output
20, 22, 26, 28, 30, 32, 38, 40	OUTn-	LVDS Output	Inverting LVDS output
19	END	Digital Input	Logic low on enable puts the LVDS data output into Tri-State and reduces supply current
42	ENCK	Digital Input	Logic low on enable puts the LVDS clock output into Tri-State and reduces supply current
12, 18, 24, 36, 43, 48	VSS	Power	Ground
1, 13, 25, 37	VDD	Power	Power supply
3	CLKIN+	LVDS Input	Non-Inverting Clock LVDS Input
2	CLKIN-	LVDS Input	Inverting Clock LVDS Input
35	CLKO+	LVDS Output	Non-Inverting Clock LVDS Output
34	CLKO-	LVDS Output	Inverting Clock LVDS Output

Table 6: Pinout description





- Notes:
1. An Index mark shall be located adjacent to Pin 1.
  2. The dimension shall be measured from the seating plane to the base plane.
  3. The true position pin spacing is 1.27mm between centerlines. Each pin centerline shall be located within  $\pm 0.13$ mm of its true longitudinal position relative to Pin 1 and the highest pin number.
  4. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
  5. The lid is electrically connected to VSS.
  6. Lead finishes are in accordance to MIL-PRF-38535.

## MARKING

The laser marked information on the component are:

- ARQUIMEA's symbol **Q**
- The Entire Part-type
- Traceability information



The traceability information comprises a manufacturing date code, a lot identification and a serial number:

- **Date Code:** Four-digit code number is used for the manufacturing date. The first two digits are the last two figures of the year of manufacture. The last two digits indicate the week of the year (i.e. 01 to 52), during which encapsulation or the final production process occurred.

- **Lot and Selected Sublot Identification:** If it is necessary to differentiate between more than one lot processed in the same week, a suffix letter (beginning with the letter A) is added to the date code. For a Selected Sublot a second suffix letter (beginning with the letter A) is added to the date code. For a single lot or sublot, letters are omitted (replaced by space).
- **Serial Number:** A serial number consisting of three digits is used. Serial numbers are run sequentially and not duplicated if more than one sub-lot is taken from one production lot.

For Engineering Models, "**EM**" marking is written after Serial Number

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## QUALITY STANDARDS

ARQUIMEA INGENIERÍA S.L.U. develops its activities under the premises of quality and sustainability, offering efficient, liable and innovative technologies and solutions to its customers.

ARQUIMEA's Quality Management System meets the requirements of ISO 9100:2010 Aerospace Series and has been audited and certified by the Spanish Association for Standardization and Certification, AENOR.



To meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in the following processes (Screened and Qualified):

- Equivalent to QML 38535 LEVEL Q or V\* (on request)
- Equivalent to ESCC 9000\*  
\*with radiation Qualification

For the procurement in die form, the following processes can be offered on request:

- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K\*

Engineering Models are available and tested at 25°C only.

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**REVISION HISTORY**

<b>Date Released</b>	<b>Issue</b>	<b>Section</b>	<b>Changes</b>
12-01-2016	Draft A	All	Initial Release copied From ARQ-LVR001 datasheet
23-09-2016	Draft B	ELECTRICAL CHARACTERISTICS	Parameter update after Electrical measurement at Room temperature
		AC SWITCHING CHARACTERISTICS	
13-02-2017	01	FEATURES, APPLICATIONS INFORMATION	Fail-safe feature not available in this version
30-10-2017	02	ELECTRICAL CHARACTERISTICS	Hysteresis feature and Failsafe Threshold Added
18-12-2017	03	TRUTH TABLE	Added table
20-02-2018	04	AVAILABLE OPTIONS	Added description, Version ARQ-LVP001-02 removed Notes Added Added Information
		PACKAGE MARKING	
01-07-2018	05	ELECTRICAL CHARACTERISTICS	Parameter update after Electrical Measurement at room temperature

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