ARQ-LVT001
RAD-HARD Dual 500Mbps Bus LVDS Transceiver

FEATURES

- Dual drivers, LVCMOS/LVTTL compatible inputs with LVDS outputs
- Dual receivers, LVDS inputs with LVCMOS/LVTTL compatible outputs
- 500.0 Mbps low jitter data path
- 3.3V single power supply
- Low power consumption
- 6mA output driver short circuit (OUT+, OUT–)
- Cold sparing on all pins
- 2ns Propagation delay in temperature range
- Extended LVDS Input Common Mode [-4; +5] V
- Receiver input threshold ≤ ± 100 mV
- 25 mV (typ) Input hysteresis
- Fail-safe protection circuit
- Radiation tolerant: 300 Krad(Si)
- Latch-up free up to 60 MeVcm^2/mg
- ESD tolerance: 8KV
- Packaging: 18-pin, Ceramic Flat Pack (CFP).
- ANSI TIA/EIA 644a LVDS standard Compliant
- Space level

DESCRIPTION

ARQUIMEA ARQ-LVT001 is a Dual BiCMOS flow-through differential line driver-receiver pair designed for aerospace applications requiring high data rates and low-power dissipation. The device is designed to support data rates above 500 Mbps utilizing Low Voltage Differential Signaling (LVDS) technology.

The drivers accept LVTTL/LVCMOS input levels and convert them to LVDS output signals. The receivers accept LVDS input signals and convert them to 3.3V LVCMOS signal levels.

In addition, the dual LVDS transceiver pair supports an individual TRI-STATE function that may be used to disable the output stages, disabling the load current, and thus dropping the device to an ultra-low idle power state.

The input buffers of LVDS receiver include an active internal fail-safe circuit that sets the output of the receiver to a known high state when one or the two inputs floating, or inputs shorted.

The extended common mode range allows high voltage drops between ground planes without affecting performance.

APPLICATIONS

The ARQ-LVT001 provides the basic bus Driver and Receiver functions that allow isolation of segments or long-distance applications.

The intended application of these devices and signaling technique is for both SpaceWire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.
The transmission media may be printed-circuit board traces, backplanes, or cables.

RADIATION HARDENING

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
TID	300	-	-	Krad	TBC
SEL	60	-	-	MeVcm^2/mg	Only validated on design ARQ-LVR001
SEE performance for a GEO orbit	1E-13 TBC	-	-	Err/Bit/day	

More information about radiation hardening features and radiation test conditions is available under request.

AVAILABLE OPTIONS

PRODUCT ORDERING Nº	QUALITY LEVEL	PACKAGE (*1)	OPERATING TEMPERATURE	VARIANT DETAIL	TERMINAL MATERIAL AND FINISH (*2)	DELIVERY PACK
ARQ-LVT001-01	Engineering Model **(*3)**	18-pin Ceramic FP	-55ºC to 125ºC	NA	D2	15-pieces tray
ARQ-LVT001S01	Space Flight Model **(*4)**	18-pin Ceramic FP	-55ºC to 125ºC	NA	D2	15-pieces tray

(*1) Other packaging options, including raw die format, are also available under request.
(*2) The terminal material and/or finish shall be in accordance with the requirements of ESCC23500
(*3) Only electrically tested at 25ºC
(*4) Space level screening and qualification per ESCC9000

INDEX

GLOSSARY

BER	*Bit Error Ratio*
CMRR	*Common Mode Rejection Ratio*
CQFP	*Ceramic Quad Flat Pack*
ESD	*Electrostatic Discharge*
GEO	*Geostationary Earth Orbit*
IC	*Integrated Circuit*
I/O	*Input/Output*
LET	*Linear Energy Transfer*
LVDS	*Low Voltage Differential Signaling*
LVTTL	*Low Voltage Transistor-Transistor Logic*
PSRR	*Power Supply Rejection Ratio*
RL	*Load Resistor*
SEE	*Single Event Effect*
SEL	*Single Event Latch-up*
TID	*Total Ionizing Dose*
tf	*Fall Time*
tr	*Rise Time*
TTL	*Transistor-Transistor Logic*
VCM	*Common-mode voltage*
VID	*Differential Input Voltage*
VOS	*Offset voltage*
VT	*Differential output voltage*

OVERVIEW

The ARQ-LVT001 provides the basic bus Driver and Receiver functions that allow isolation of segments or long-distance applications. The intended application of these devices and signaling technique is for both space-wire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

BLOCK DIAGRAM

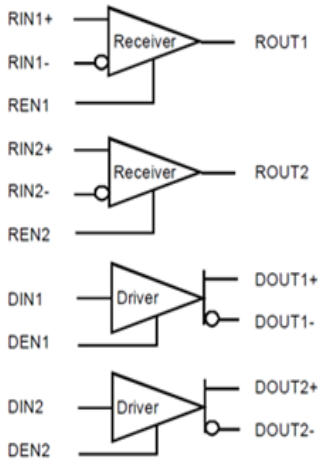


Figure 1: Block diagram

TRUTH TABLE

MODE	ENABLES (*)	INPUTS	OUTPUTS	
	DEN	DIN	DOUT+	DOUT-
Disabled	L	X	Z	Z
Enabled	H	L	L	H
	H	H	H	L
	H	OPEN	L	H

Table 1: Driver Truth table

MODE	ENABLES (*)	INPUTS	OUTPUTS
	REN	$V_{ID} = V_{RIN+} - V_{RIN-}$	ROUT
Disabled	L	X	Z
Enabled	H	$V_{ID} > V_{TH}$	H
	H	$V_{TL} < V_{ID} < V_{TH}$	?
	H	$V_{ID} < V_{TL}$	L
Fail-Safe	H	OPEN/SC/Terminated for tFS>500ns	H

Table 2: Receiver Truth table

Notes:
(*) If the enable input is left floating the circuit is enabled.
(**) L= low Logic Level, H= High Logic Level, X= Irrelevant, Z= High Impedance, '?'=Indeterminate

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V_{DD}	DC supply voltage	-0.5 to 4.6V
V_I	TTL/CMOS Input Voltage	-0.5V to 6V
V_{IN}	LVDS Input Voltage	-5V to 6V
T_{STG}	Storage temperature	-65 to +150^{O}C
T_J	Maximum junction temperature	+175^{O}C
Tc	Maximum Case temperature	+125ºC
ESD	ESD Last Passing Voltage – HBM	8kV
P_D	Power dissipation	1,25W

Table 3: Absolute Maximum Rating

Note: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating as well as derated Conditions according to ECSS-Q-30-11A are presented below

SYMBOL	PARAMETER	OPERATING VALUES	DERATED VALUES
V_{DD}	Power supply voltage	3.0 to 3.6V	3.0 to 3.6V
V_{IN}	TTL/CMOS Input Voltage	0 to 5V	0 to 5V
	LVDS input voltage, receiver inputs	-4.6V to 5.6V	-4.6V to 5.6V
V_{CM}	LVDS Input Common Mode Voltage	-4V to 5V	-4V to 5V
T_C	Case temperature range	-55 to +125 ^{O}C	+100ºC (Tj=110ºC)

Table 4: Recommended Operating Conditions

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, -55°C < TC < +125°C

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
TTL/CMOS DC SPECIFICATIONS (REN, DEN, DIN)					
V_{IH}	High-level input voltage		2.0	5V	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_{IH}	High-level input current	V_{IN} = 3.6V; V_{DD} = 3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN} = 0V; V_{DD} = 3.6V	-10	+10	µA
I_{CS}	Cold Spare Leakage current	V_{IN} = 3.6V, V_{DD} = V_{SS}	-3,6	+3,6	µA
TTL/CMOS OUTPUT DC SPECIFICATIONS (OUT)					
V_{OH}	High-level output voltage	IOH = -0.4mA, V_{DD} = 3.0V	2.4	V_{DD}	V
		IOH = -2mA, V_{DD} = 3.0V	2.2	V_{DD}	V
V_{OL}	Low-level output voltage	IOL = 2mA, V_{DD} = 3.0V	-0.3	0.4	V
I_{CS}	Cold Spare Leakage current	V_{IN} = 3.6 V, V_{DD} = V_{SS}	-6	+6	µA
I_{OZ}	Output Tri-State Current	Tri-State output (channel disabled), V_{OUT} = V_{DD} or V_{SS}	-20	+20	µA
I_{OS}	Output Short Circuit Current (Only one output should be shorted at a time)	V_{OUT} = 0 V		-50	mA
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)					
V_{OD}	Differential Output Voltage	R_L = 100Ω	247	453	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	R_L = 100Ω		10	mV
V_{OS}	Offset Voltage	R_L = 100Ω $V_{OS} = \frac{V_{OH}+V_{OL}}{2}$	1.125	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	R_L = 100Ω		50	mV
ΔV_{OSB}	Imbalance of Differential Offset Voltage during Voltage transition	R_L = 100Ω, C_L = 1pf to 10pf		150	mV
I_{OZ}	Output Tri-State Current	Tri-State output (channel disabled), V_{OUT} = V_{DD} or V_{SS}	-5	+5	µA
I_{CSOUT}	Cold Sparing Leakage Current	V_{OUT} = 3.6V, V_{DD} = V_{SS}	-5	+5	µA
I_{OS}	Output Short Circuit Current (Only one output should be shorted at a time)	V_{OUT+}=V_{OUT-}=0V	6		mA
		V_{OUT+}=V_{OUT-}	4		mA
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)					
V_{TH}	Differential Input High Threshold	V_{CM} = -4V to +5V	+100	+600	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = -4V to +5V	-600	-100	mV
V_{ID_HYS}	Differential Input hysteresis	V_{CM} = -4V to +5V	20		mV
V_{ID_FS}	Differential Input Fail-safe threshold	Low Differential Threshold voltage or Open circuit maintained more than 500ns	20		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 350 mV	-4	+5	V
I_{IN}	Input Current	V_{DD} = +3.6V, V_{CM} = -4V to +5V, V_{IN+}=V_{TLmin}, V_{IN-}=V_{THmax}	-10	+10	µA
		V_{DD} = +3.6V, V_{CM} = -4V to +5V, V_{IN-}= V_{TLmin}, V_{IN+}=V_{THmax}	-10	+10	µA
ΔI_{IN}	Input Current Balance (I_{IN+}-I_{IN-})	V_{DD} = +3.6V, V_{CM} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CM}	-6	6	µA
I_{CSIN}	Cold Sparing Leakage Current	V_{IN} = +3.6V, V_{DD} = V_{SS}	-20	+20	µA
C_{IN}	Input Capacitance			3	pF
SUPPLY CURRENT					
I_{CLLS}	Total Supply Current	END/ENR=V_{DD}, V_{DD} = 3.6 V, Fq = DC Driver: R_L = 100 Ω Receiver: No Load		45	mA
I_{CCZ}	Tri-State Supply Current	END, ENR = V_{SS}, V_{DD} = 3.6V		10	mA
PSRR	Driver Power Supply Rejection Ratio	R_L=100Ω, END=V_{DD}, V_{DD}=3.6V, Fq=250MHz		-50	dB

Table 5: DC Electrical Characteristics

AC SWITCHING CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, TA = -55°C to +125°C.

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
LVDS DRIVER					
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	R_L = 100 Ω, C_L = 10 pf		4.5	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	R_L = 100 Ω, C_L = 10 pf		4.5	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	R_L = 100 Ω, C_L = 10 pf		250	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	R_L = 100 Ω, C_L = 10 pf		250	ns
t_{LHT}	Input/Output Low-to-High Transition Time, 20% to 80%	R_L = 100 Ω, C_L = 1 pf to 10 pf	260	600	ps
t_{HLT}	Input/Output High-to-Low Transition Time, 80% to 20%	R_L = 100 Ω, C_L = 1 pf to 10 pf	260	600	ps
t_{PLHD}	Propagation Low to High Delay	R_L = 100 Ω, C_L = 10pf		2	ns
t_{PHLD}	Propagation High to Low Delay	R_L = 100 Ω, C_L = 10pf		2	ns
T_{SKEW}	Differential Skew t_{PHLD} - t_{PLHD}	R_L = 100 Ω, C_L = 10pf		150	ps
T_{CCS}	Output Channel-to-Channel Skew	R_L = 100 Ω, C_L = 10pf		500	ps
T_{DDS}	Output Device-to-Device Skew	R_L = 100 Ω, C_L = 10pf		750	ps
t_{PJ}	Periodic Jitter	50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		15	ps
t_{CCJ}	Cycle to Cycle Jitter	50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		40	ps
t_{PPJ}	Peak to Peak Jitter	V_{IN} = 2^(7)-1PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		250	ps
t_{DJ}	Deterministic Jitter	V_{IN} = 2^(7)-1PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		200	ps
LVDS RECEIVER					
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	C_L = 10 pf		4.5	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	C_L = 10 pf		4.5	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	C_L = 10 pf		250	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	C_L = 10 pf		250	ns
t_{LHT}	Rise Time, 20% to 80%	C_L = 10pf	800		ps
t_{HLT}	Fall Time, 80% to 20%	C_L = 10pf	800		ps
t_{PLHD}	Propagation Low to High Delay	C_L = 10 pf		2	ns
T_{PHLD}	Propagation High to Low Delay	C_L = 10 pf		2	ns
T_{SKEW}	Differential Skew T_{PHLD} - T_{PLHD}			300	ps
T_{CCS}	Output Channel-to-Channel Skew			500	ps
T_{DDS}	Output Device-to-Device Skew			750	ps
t_{PJ}	Periodic Jitter	V_{ID} = 200mV, 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		15	ps
t_{CCJ}	Cycle to Cycle Jitter	V_{ID} = 200mV, 50% duty cycle at 250MHz, trise≤ 1ns (20% - 80%)		40	ps
t_{PPJ}	Peak to Peak Jitter	V_{ID} = 2^(7)-1PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		250	ps
t_{DJ}	Deterministic Jitter	V_{ID} = 2^(7)-1PRBS pattern at 500Mbps, trise ≤ 1ns (20% - 80%)		200	ps

Table 6: AC Electrical Characteristics

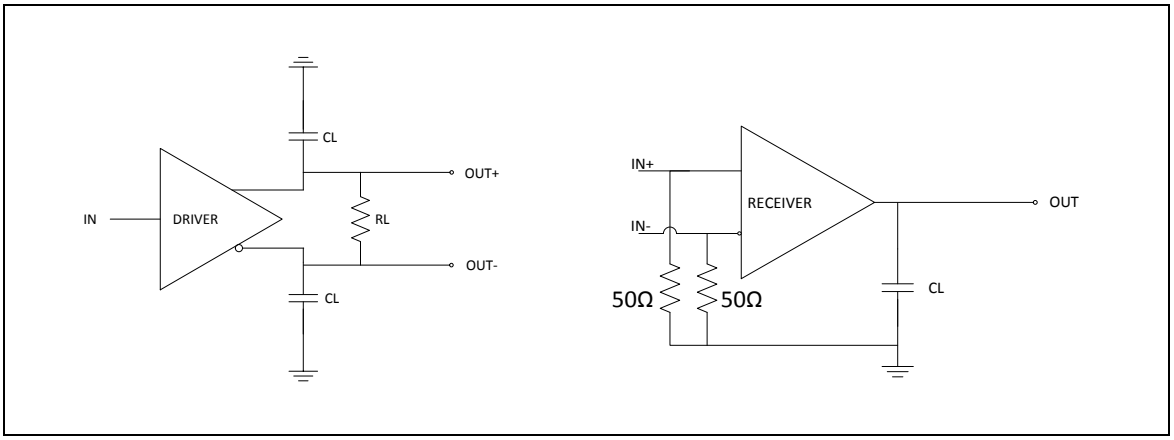


Figure 2: LVDS Output load

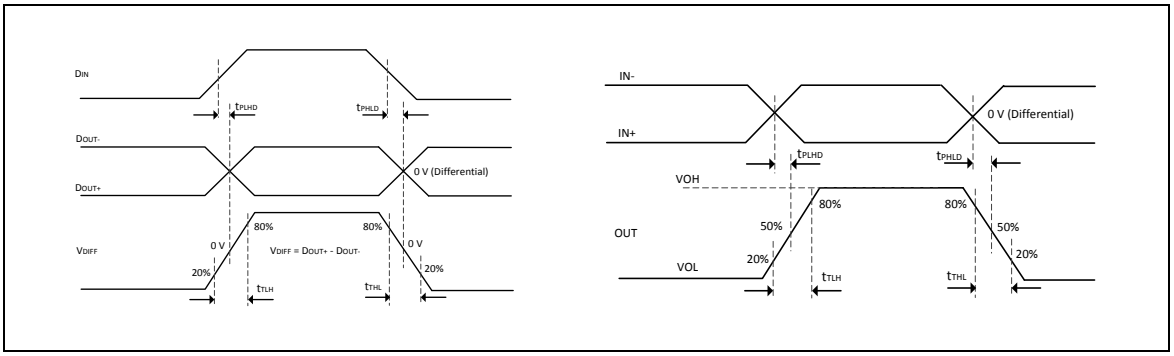


Figure 3: LVDS Propagation delay and transition time (Left: LVDS Driver, Right: LVDS Receiver)

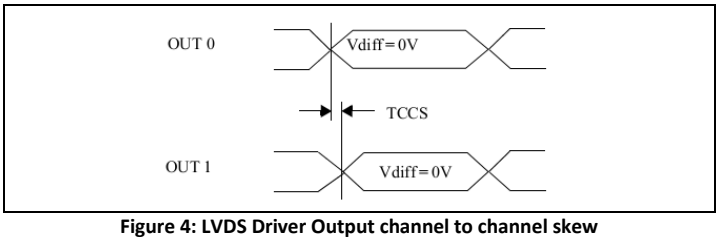


Figure 4: LVDS Driver Output channel to channel skew

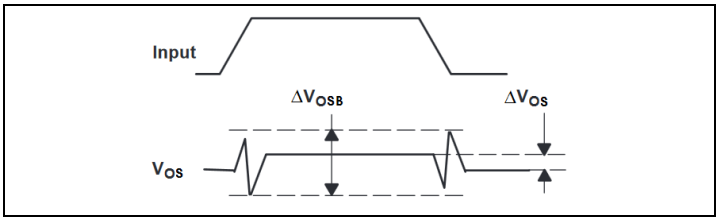


Figure 5: LVDS Offset Voltage

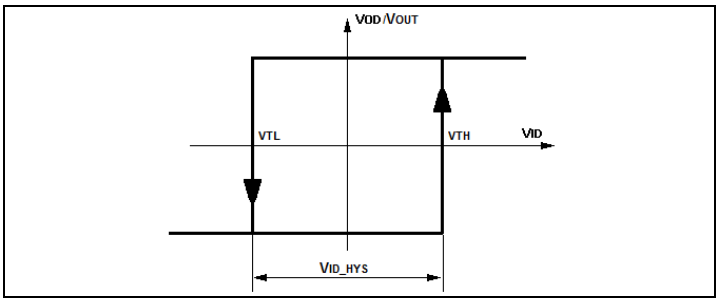
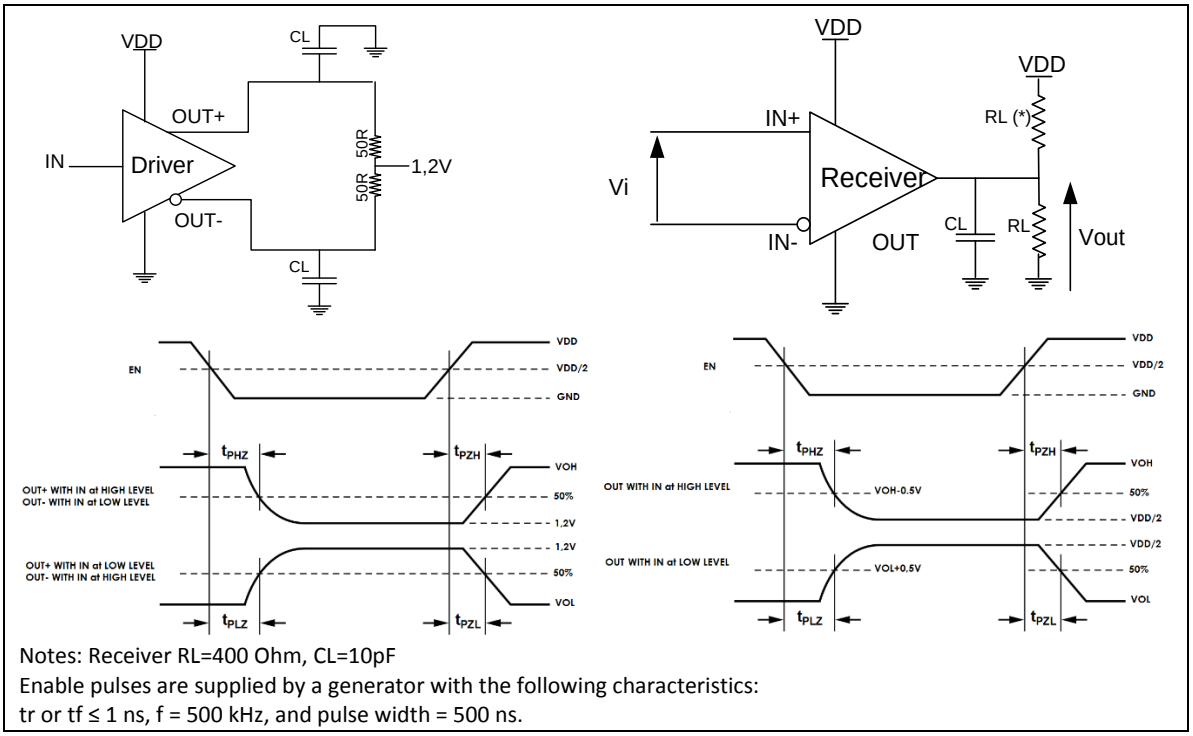


Figure 6: LVDS Receiver Input Differential Hysteresis



Notes: Receiver RL=400 Ohm, CL=10pF
Enable pulses are supplied by a generator with the following characteristics:
tr or tf ≤ 1 ns, f = 500 kHz, and pulse width = 500 ns.

Figure 7: Output active to TRISTATE and TRISTATE to active (Left: LVDS Driver, Right: LVDS Receiver)

APPLICATIONS INFORMATION

Transmission media:

The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The signal path should be matched in length to avoid any skew in differential lines or between channels.

Input Fail-Safe (comparator and timer)**:**

The ARQ-LVT001 also supports Fail-Safe operation when OPEN or SHORTED inputs are present. Receiver output goes HIGH after 500ns for all fail-safe conditions.

PCB layout and Power System Bypass:

Circuit board layout and stack-up for the ARQ-LVT001 should be designed to provide noise-free power to the device.

Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. A 0.25Ohm resistor is recommended in the power supply line path. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use value of 0.1µF. Tantalum capacitors may be 2.2µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the ARQ-LVT001, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

TYPICAL APPLICATION

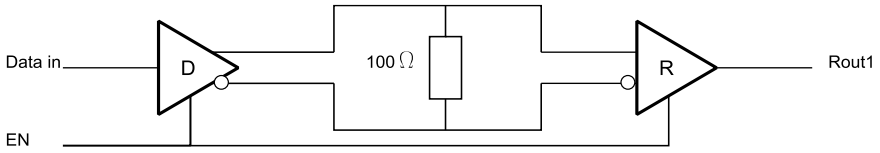


Figure 8: Point to Point Typical Application

PINOUT DESCRIPTION

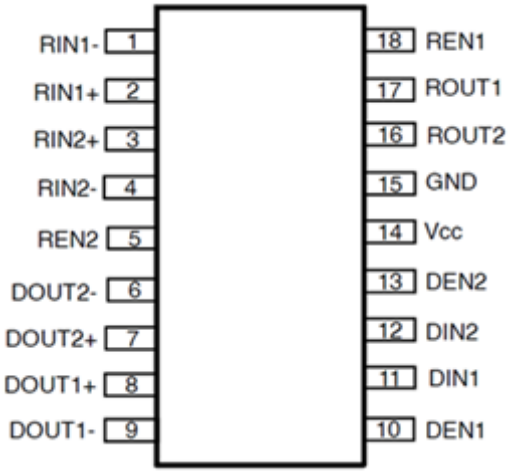


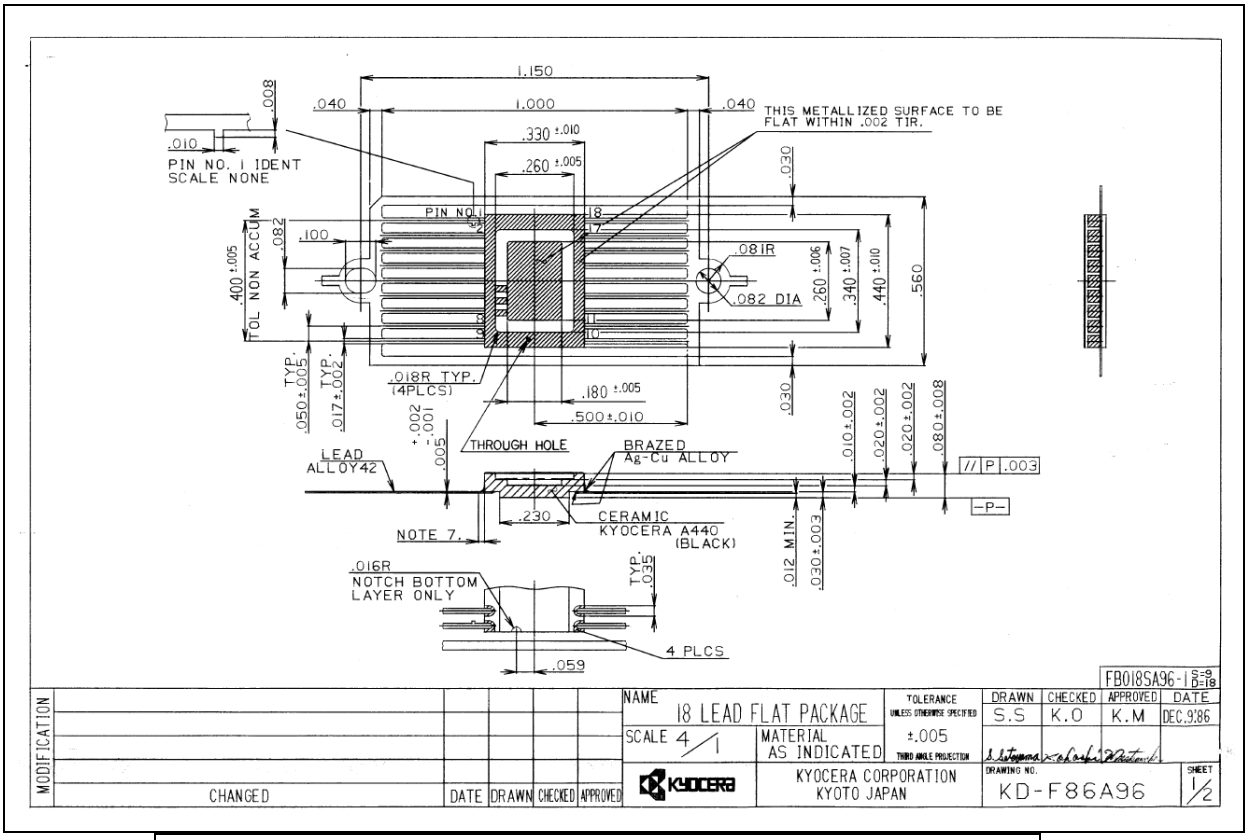
Figure 9: Pinout diagram

Pin Nº	Name	Type	Description
1 (F)	RIN1-	LVDS Input	Inverting LVDS input
2	RIN1+	LVDS Input	Non-Inverting LVDS input
3	RIN2+	LVDS Input	Non-Inverting LVDS input
4	RIN2-	LVDS Input	Inverting LVDS input
5	REN2	Digital Input	Logic low on enable switch-off the LVDS receiver
6	DOUT2-	LVDS Output	Inverting LVDS output
7	DOUT2+	LVDS Output	Non-Inverting LVDS output
8	DOUT1+	LVDS Output	Non-Inverting LVDS output
9	DOUT1-	LVDS Output	Inverting LVDS output
10	DEN1	Digital Input	Logic low on enable puts the LVDS clock output into Tri- State and reduces supply current
11	DIN1	Digital Input	CMOS/TTL input
12	DIN2	Digital Input	CMOS/TTL input
13	DEN2	Digital Input	Logic low on enable puts the LVDS clock output into Tri- State and reduces supply current
14	VCC	Power	Power supply
15	GND	Power	Power supply
16	ROUT2	Digital Output	CMOS/TTL output
17	ROUT1	Digital Output	CMOS/TTL output
18	REN1	Digital Input	Logic low on enable switch-off the LVDS receiver

Table 7: Pinout Description

PACKAGE

FP-18 Drawing



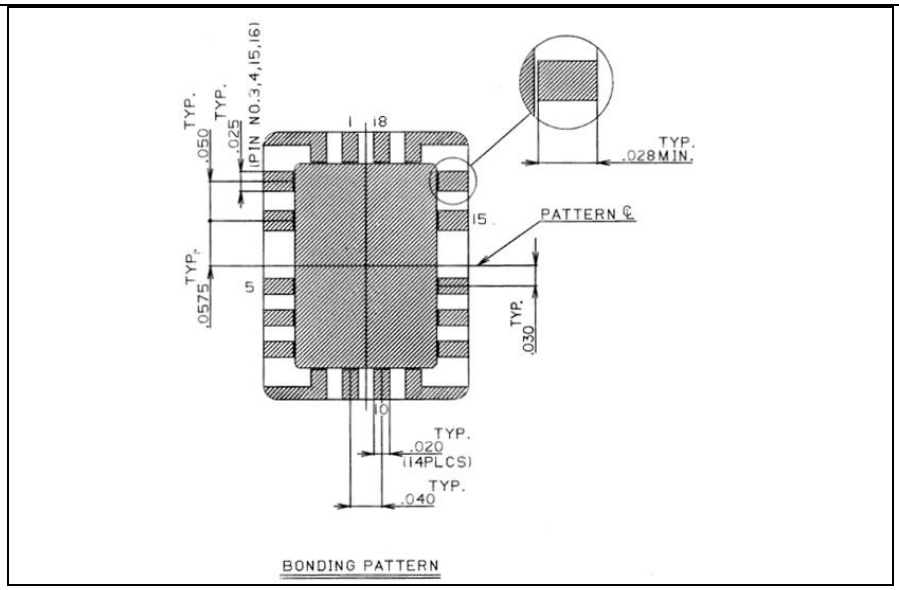


Figure 10: FP-18 Package drawing

Notes:
1. An Index mark shall be located adjacent to Pin 1.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centerlines. Each pin centerline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
5. The lid is electrically connected to VSS.
6. Lead finishes are in accordance to MIL-PRF-38535.

MARKING

The laser marked information on the component are:

- ARQUIMEA's symbol **Q**
- The Entire Part-type
- Traceability information

The traceability information comprises a manufacturing date code, a lot identification and a serial number:

- **Date Code**: Four-digit code number is used for the manufacturing date. The first two digits are the last two figures of the year of manufacture. The last two digits indicate the week of the year (i.e. 01 to 52), during which encapsulation or the final production process occurred.

- **Lot and Selected Sublot Identification**: If it is necessary to differentiate between more than one lot processed in the same week, a suffix letter (beginning with the letter A) is added to the date code. For a Selected Sublot a second suffix letter (beginning with the letter A) is added to the date code. For a single lot or sublot, letters are omitted (replaced by space).
- **Serial Number**: A serial number consisting of three digits is used. Serial numbers are run sequentially and not duplicated if more than one sub-lot is taken from one production lot.

For Engineering Models, "**EM**" marking is written after Serial Number

QUALITY STANDARDS

ARQUIMEA INGENIERÍA S.L.U. develops its activities under the premises of quality and sustainability, offering efficient, liable and innovative technologies and solutions to its customers.

ARQUIMEA's Quality Management System meets the requirements of ISO 9100:2010 Aerospace Series and has been audited and certified by the Spanish Association for Standardization and Certification, AENOR.

To meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in the following processes (Screened and Qualified):

- Equivalent to QML 38535 LEVEL Q or V* (on request)
- Equivalent to ESCC 9000*

  *with radiation Qualification

For the procurement in die form, the following processes can be offered on request:

- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K*

Engineering Models are available and tested at 25ºC only.

IMPORTANT NOTICE

ARQUIMEA INGENIERÍA S.L.U. and its subsidiaries (ARQUIMEA) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers must obtain the latest relevant information before placing orders and must verify that such information is current and complete. All products are sold subject to ARQUIMEA's terms and conditions of sale supplied at the time of order acknowledgment.

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REVISION HISTORY

Date Released	Issue	Section	Changes
20-09-2017	Draft A	All	Initial Release
30-10-2017	01	All	Format change
28-11-2017	02	TRUTH TABLE	Added table
20-02-2018	03	AVAILABLE OPTIONS PACKAGE MARKING	Added description Notes Added Added Information
01-07-2018	04	ELECTRICAL CHARACTERISTICS	Parameter update after electrical measurements at room

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